OFFICE INTERFACE UNIT FOR DDS (OIU/DDS), 628095

GENERAL DESCRIPTION

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1. GENERAL

1.01 This Section provides a general description of the ITT D448 office interface unit for DDS® (OIU/DDS), 628095 (Fig. 1), to the functional block diagram level.

1.02 Whenever this Section is reissued, the reasons for reissue will be listed in this paragraph.

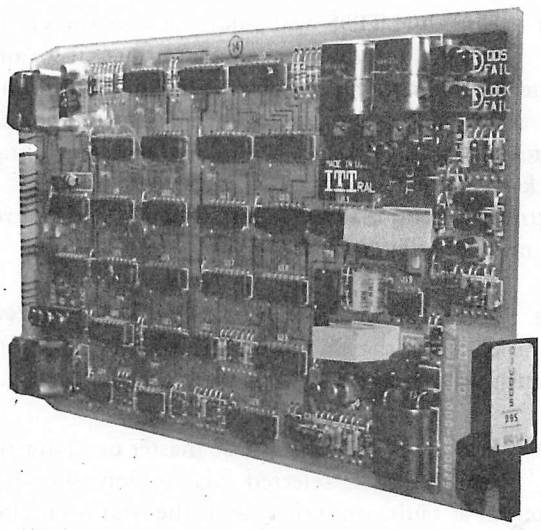

Fig. 1—OIU/DDS, 628095

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1.03 The OIU/DDS supports ITT D448 dataports by allowing a D448 multiplex terminal to synchronize to a customer-selected timing source, thereby permitting synchronous data transmission.

1.04 The OIU/DDS has four customer-selected timing options. The unit will phase-lock:

(a) The transmit clocks of both digroups to the receive clock of the A digroup by selecting option screw [A] (loop timing mode A);

(b) The transmit clocks of both digroups to the receive clock of the B digroup by selecting option screw [B] (loop timing mode B);

(c) The transmit clocks of both digroups to an external office clock by selecting option screw [DDS] (DDS clock timing mode); or

(d) The transmit clock of the A digroup to the transmit clock of the B digroup by selecting option screw [LOC] (master oscillator mode).

Note 1: The OIU/DDS incorporates all of the same functions as the OIU for loop timing (OIU/LT), 628090, and can be used interchangeably if loop timing only is required.

Note 2: The OIU/DDS can be used in Group -002 and later issue D448 mulitplex shelves only.

2. DESCRIPTION

2.01 The unit mounts in the OIU common unit position in the D448 multiplex shelf. Installation procedures are provided in Section ITTR-18-442.

2.02 The unit is available in Group -001 only.

2.03 The unit consists of an epoxy-glass printed circuit board (PCB) and associated circuit components. The lower front edge of the PCB is fitted with a handle to facilitate insertion and removal of the unit from the shelf. An identification strip on the handle face indicates the unit mnemonic (OIU/DDS), part number, and issue letter. The mnemonic, part number, and issue letter are also located on the component side of the PCB.

2.04 The DDS FAIL (DS1) and LOCK FAIL (DS2) LEDs are located on the front edge of the PCB.

2.05 Printed circuit wiring is etched on both sides of the PCB. The unit inputs and outputs terminate in gold-plated contacts on the rear edge of the PCB. These contacts mate with a 70-pin contact card edge connector on the rear of the multiplex shelf.

3. FUNCTIONAL OPERATION (FIG. 2)

3.01 The DDS-format office clock (64.0 kb/s ± 100 ppm maximum, shown in Fig. 3) enters the OIU/DDS on the DDSCLKI tip/ring leads. This AMI clock signal is then converted to a unipolar 64.0 kb/s TTL-compatible signal via the AMI-to-TTL converter. This unipolar signal is then sent to the bit/byte marker generator, which generates the external BIT and BYTE MARKER signals. The signal BIT is the TTL decode of the DDS clock and is used by the data test interface (DTI). The signal BYTE MARKER is the TTL decode of the DDS clock bipolar violations and is also used by the DTI.

3.02 The clock detectors monitor the DDS clock and the digroup B transmit clock for pulses. If there is a failure of one (or both) of the clocks, the clock detectors will turn on the DDS FAIL LED (DS1) and signal the control circuit to take appropriate action.

3.03 The phase lock select circuit is under control of the control circuit. Depending on the output of the control circuit, the phase lock select circuit will output the proper signals to the phase-locked loops.

3.04 Phase-locked loop #1 phase locks the transmit clock (TCL1544L) to the reference signal output of the phase lock select circuit (DDS, receive clock, or master transmit clock). The customer must select the proper option screw [T1] or [T1C] (p/o option block E1) for the mode of operation being used. For Mode 1 operation, option screw [T1C] should be selected. For Modes 2 or 3, option screw [T1] should be selected. The output signal (TCL1544L) is used by the line interfaces (LIs) instead of their internal oscillator, depending on the value of SELECTA and SELECTB.

3.05 Phase-locked loop #2 is used to generate the signals DCL1344A and DCL1344B. These outputs are used by the OCUDP and DS0DP channel units. These outputs are also used by the divide-by-168 circuit to produce DS0CLA, DS0CLB, and the TTL signals to the TTL-to-AMI converter.

3.06 The TTL-to-AMI converter converts the TTL signals from the divide-by-168 circuit to an AMI signal (DDSCLKO tip/ring) for use by the OCUDP and DS0DP channel units. This clock is the TTL-encoded DDS clock.

3.07 The select control circuit controls the SELECTA and SELECTB output lines. These lines control whether the LIs use their internal oscillator for TCL1544 or use TCL1544L instead.

3.08 The control circuit controls the overall operation of the OIU/DDS. It monitors the alarm lines and customer-selected options and causes the phase lock select circuit to output the proper signals to each phase-locked loop.

4. OPTIONS

4.01 The OIU/DDS is equipped with six screw-down options which allow the unit to be configured for different applications. Option screws [A], [B], [DDS], and [LOC] are described in Para. 1.04 of this Section. The option screws [T1] and [T1C] are used to select the appropriate internal crystal oscillator to be used by phase-locked loop #1 for the different modes of D448 multiplex terminal operation. The unit is shipped with option screws [DDS] and [T1] factory-selected (down). Option selection procedures are provided in Section ITTR-18-442.

5. SPECIAL FEATURES AND RESTRICTIONS

5.01 The OIU/DDS will phase-lock to the customer-selected option unless an alarm forces it to another source. If the selected option is loop timing (option screw [A] or [B] down) and there is an alarm in the selected digroup, the OIU/DDS will phase-lock both transmit clocks to the receive clock of the alternate digroup. If the alternate digroup is also in alarm, the OIU/DDS reverts to the master oscillator timing mode.

5.02 If the OIU/DDS is phase-locked to the DDS office clock and the DDS office clock fails, the OIU/DDS reverts to the master oscillator timing mode.

5.03 If the OIU/DDS is in the master oscillator timing mode either selected via option selection or through a fault condition and the transmit clock of digroup B fails, the OIU/DDS does not attempt to phase-lock to any signal and operates in a free-running mode.

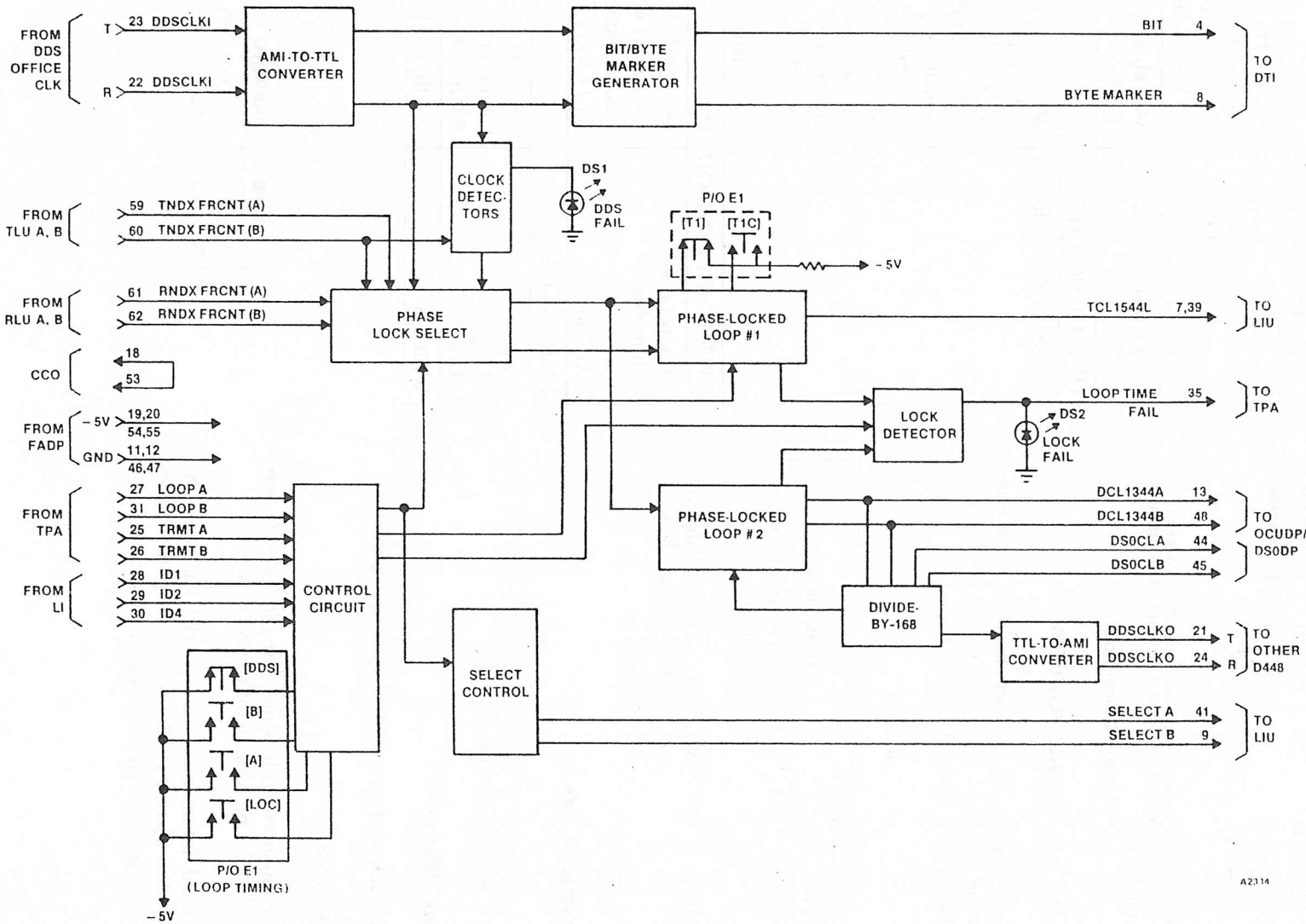
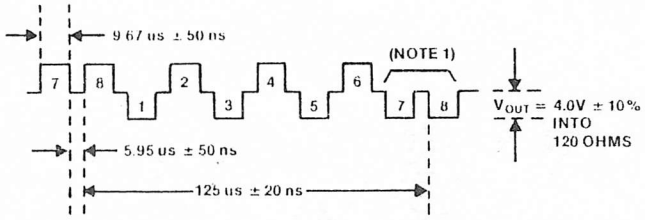


Fig 2—OIU/DDS, 628095, Functional Block Diagram



NOTES:
1. PULSES ALTERNATE IN POLARITY ACCORDING TO BIPOLAR RULE, EXCEPT FOR 8TH BIT. THE 8TH BIT IS ALWAYS THE SAME POLARITY AS THE 7TH BIT.

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Fig. 3—DDS Office Clock

6. TEST AND MAINTENANCE FEATURES

6.01 A description of the test and maintenance features on the unit is provided in Table A. Refer to Fig. 1 for the physical location of these features.

TABLE A

FEATURE	REF. DES.	FUNCTION
DDS FAIL LED	DS1	When on, indicates failure of DDS office clock.
LOCK FAIL LED	DS2	When on, indicates failure of OIU/DDS to phase-lock to incoming clock.

7. TECHNICAL SUMMARY

7.01 A summary of the technical specifications of the unit is given in Table B.

8. REPLACEABLE PARTS

8.01 The unit contains no field-replaceable parts.

9. REFERENCES

9.01 The engineering drawings noted in Table C were used in the preparation of this Section.

9.02 Related information on the OIU/DDS may be found in Section ITTR-18-442, Dataport Channel Units — Option Selection and Installation.

TABLE B

ITEM	SPECIFICATION
INPUT POWER	
Voltage −5 ±0.25 Vdc −17 ±0.75 Vdc +7 ±0.75 Vdc	Current Drain 720.5 mA (maximum) 6.0 mA (maximum) 6.0 mA (maximum)
DDS CLOCK INPUT	64.0 kb/s ± 100 ppm (maximum)
OUTPUT SIGNALS	
DDSCLKO Tip/Ring	When terminated by 120 ohms ± 15% with no cable, the output will be 8 Vpp ± 10%. When terminated by four 24AWG twisted, shielded pair cables of 0 to 1500 ft terminated in up to 7 OIU/DDSs and one 150-ohm resistive load per cable, the output will be 2.0V (nominal).
OPERATING ENVIRONMENT	
Temperature Humidity Altitude	0° to 55°C To 95% at 40°C (no condensation) To 14,000 ft (4,300 m)
DIMENSIONS	
Width Height Depth	0.5 in. (1.3 cm) 5.0 in. (12.7 cm) 9.6 in.(24.4 cm)
WEIGHT	0.4 lb (0.2 kg)

TABLE C

TYPE	DRAWING NO.
Assembly Schematic	628095-000 628095-002